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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
HEIN, GREGORY P	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 12/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/669,886	URARD, PASCAL	
	Examiner	Art Unit	
	Gregory P. Hein	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3 - 4,15 - 16, 18 - 21* is/are rejected.

7)☒ Claim(s) *2, 6 - 10, 12 - 13, 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 3/25/2004 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Drawings

2. The drawings submitted on 9/24/2003 are approved by the examiner.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 5, 11 and 14 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

5. Claim 5 claims a deferred memory. However, the specification does not adequately describe this structure and its operation to enable one of ordinary skill in the art.

Claim 11 claims an instant read memory. However, the specification does not adequately describe the structure and operation to enable one of ordinary skill in the art.

Claim 11, line 66 claims a multiplexer instantaneously reproducing output from the memories. Due to intrinsic gate delay an instantaneous reproduction of input on the output of a multiplexer is not possible.

Claim 14 claims an instant memory receiving command and address input in a clock cycle and reproducing the corresponding data in the same clock cycle. The specification does not adequately describe this structure and its operation to enable one of ordinary skill in the art.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 3 – 4, 15 – 16, 18 - 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,287,309 (Kai) and further in view of U.S. Patent 6,178,472 (Carpenter).

As per claim 1:

Kai teaches two random access memories (RAM) (Kai Col. 4 lines 27 – 30) with data inputs connected to a data source, command and address inputs, and outputs

(Col. 4 lines 40 – 45). Per the 2^{N+1} memory locations, RAM memories are addressed using binary code. The nature of binary code necessitates memory addresses on the order of multiples of 2.

Kai teaches multiplexing means having first and second data inputs connected to RAM memories (Kai Col. 5 lines 52 - 55).

Kai does not disclose a third input to the multiplexing means connected to the data source.

Carpenter discloses a bypass multiplexer. The bypass multiplexer allows data to pass immediately from the data source to the output of the multiplexer (Carpenter Col. 4 lines 56 – 67 and Fig. 3 #90). This multiplexing means allows selection of data from either one of the two RAM's or the data source. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Carpenter to Kai since Carpenter provides "...an improved queue within a digital circuit" (Carpenter Col. 2 lines 1 – 2).

Kai teaches a controller issuing electrical signals. The stack pointer is equivalent to applicant's controller. It generates the addresses required for simultaneous RAM read/write operations (Kai Col. 4 lines 58 – 63). The least significant bit (LSB) of the address, generated at the stack pointer, is removed and sent to the RAM's for access control (Kai Col. 5 lines 36 – 44). The removed LSB also acts as the switching command for the multiplexing means (Kai Col. 5 lines 52 – 55).

Kai discloses alternating simultaneous read/write access commands between the RAM's (Kai Col. 4 lines 50 - 53).

Kai discloses storing data into RAM in a successive order where all data preceding the current read/write address is valid (Kai Col. 2 lines 56 – 58). The structure disclosed by Kai is a LIFO stack. The method of reading data in a numerically reversed accessed way is inherent to a LIFO system and is implied by Kai's LIFO disclosure.

Applicant discloses data stored into the RAM from data source is chronologically reversed. This type of data reorganization is inherent to a LIFO stack and is in common use by those of ordinary skill in the art.

As per claim 3:

The RAM disclosed in the claim 1 has 2^{N-1} storage locations. To address all the storage locations a minimum of N – 1 bits are required. It is inherent to the system that the device is configured to code the address over N – 1 bits.

As per claim 4:

Kai does not teach a means for sampling the output of the multiplexer.

Carpenter discloses sampling the output of the multiplexer using a D flip-flop.

Kai discloses the structure of claim 1 and carpenter discloses sampling the output of a multiplexer using a D flip-flop (Carpenter Fig. 1 #18). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Carpenter to Kai for the same reasons as given in claim 1.

As per claim 15:

Kai teaches issuing data from a source to two RAM's each receiving data from a common source (Kai Col. 4 lines 27 – 33).

Kai does not teach a multiplexer directly connected to the RAM output and the data source.

Carpenter teaches a bypass multiplexer connected to the stack output and the data source such that the controller can select between the data source and the stack output (Carpenter Col. 4 lines 56 – 67 and Fig. 3 #92). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Carpenter to Kai since Carpenter provides "...an improved queue within a digital circuit" (Carpenter Col. 2 lines 1 – 2).

Kai teaches alternating simultaneous read and write commands to each of the memories (Kai Col. 4 lines 46 – 57 teach issuing a POP command on one memory bank while simultaneously issuing a PUSH command on the other memory bank. A POP command is equivalent to a read and a PUSH command is equivalent to a write.)

Kai teaches issuing addresses during the sequence so that each memory bank receives the same address (Kai Col. 5 lines 45 – 51 teach a stack incrementer/decrementer. Additionally, Kai Col. 2 line 56 – Col. 3 line 5 teach storing data into the memory banks in an ascending order.)

As per claim 16:

Kai teaches two RAM's with data inputs connected to a source, with command and address inputs and an output (Kai Col. 4 lines 27 – 33.)

Kai also teaches a multiplexer with an output and first and second inputs connected to the memory outputs (Kai Col. 5 lines 52 – 55 refer to a selector selecting between the two disclosed memory bank outputs according to a select signal.)

Kai teaches a controller issuing electrical signals. The stack pointer is equivalent to applicant's controller. It generates the addresses required for simultaneous RAM read/write operations (Kai Col. 4 lines 58 – 63). The least significant bit (LSB) of the address, generated at the stack pointer, is removed and sent to the RAM's for access control (Kai Col. 5 lines 36 – 44). The removed LSB also acts as the switching command for the multiplexing means (Kai Col. 5 lines 52 – 55). Additionally, Kai discloses the stack pointer controlling the read/write commands for simultaneous read/write operations (Kai Col. 2 lines 4 – 17.)

Kai does not teach a logic device attached to the output of the multiplexer to sample the output.

Carpenter teaches a D flip-flop attached to the output of a multiplexer.

The D flip-flop is attached to the output of stack. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Carpenter to Kai since Carpenter provides "...an improved queue within a digital circuit" in Carpenter Col. 2 lines 1 – 2 and shown in Fig. 3)

Kai teaches simultaneous alternate read/write command signals to the two RAM's (Kai Col. 4 lines 46 – 57).

Kai teaches sending address signals to the RAM's in an increasing sequence followed by a decreasing sequence (Kai Col. 5 lines 45 - 51.)

Kai teaches multiplexing the output of the RAM's so that the multiplexer selects between one of the two memory bank outputs (Kai Col. 5 lines 52 – 55.)

As per claim 18:

Kai teaches alternating writing received data into a first and a second memory (Kai Col. 2 lines 56 – 63.)

Kai teaches alternating reading between the first and second memories (Kai Col. 4 lines 40 – 57.)

Kai teaches selecting addresses in a sequentially increasing and sequentially decreasing method (Kai Col. 5 lines 45 – 51.)

As per claim 19:

Kai teaches alternating reads and writes while simultaneously sequentially incrementing addresses followed by sequentially decrementing addresses (Kai Col. 5 lines 45 – 51.)

As per claim 20:

Kai teaches a selector that alternates output based on the least significant bit between the two memory blocks (Kai Col. 5 lines 52 – 62.)

As per claim 21:

Kai is directed to methods of improving stack memories. Kai Col. 1 lines 9 – 12 make clear that the disclosure is also directed to improving LIFO memories. It is inherent to a LIFO stack that the data in the stack is read in a chronologically reversed order from the order in which data reads occurred.

Allowable Subject Matter

8. Claims 2, 6 – 10, 12 - 13, 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. As per claims 6 and 17, Kai does not teach the same or an equivalent structure as the second multiplexer with two inputs respectively attached to the first multiplexer output and the data source. While the architecture is not novel, no art with adequate motivation to combine with Kai for obviousness could be found.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gregory P. Hein whose telephone number is 571-272-4180. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mano Padmanabhan 12/12/05

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER

12/1/2005
Gregory Hein